

[0044] In one embodiment, the frequency multiplier 142 is a PLL with a phase detector 144, a loop filter 145, a voltage controlled oscillator (“VCO”) 146, a reference divider 147, and a feedback divider 148. A low-pass filter (LPF) can be used to remove high frequency components from an error signal generated by the phase detector. The oscillation frequency of the VCO is controlled with the smoothed error signal to tune its output frequency to the input data. A fixed reference signal is transmitted to the reference divider 147 and then to one input of the phase detector 144. The output of the VCO 146 is divided by the feedback divider 148 and input to the other input of the phase detector 144. Although the frequency at the output of this implementation of the frequency multiplier 142 is an integer multiple of the

[0048] Turning now to FIG. 3, a plurality of processing units operates in parallel. This embodiment relies on varying the clock signals to control power consumption. Each of the processing units 310, 312, 314, 316 and 318 is powered by the same voltage rail. A master clock 302 supplies a master clock signal to a clock controller 304. The clock controller 304 determines for each application the appropriate clock signal that is applied to each of processing units 310, 312, 314, 316 and 318. The controller 304 drives the clock input of each of processing units 310, 312, 314, 316 and 318. The clock can be driven independently and can be based on the tasks to be performed. For example, a task-based clock scheme for an exemplary three-processor system at a particular time point is as follows:

Processor	Task 1	Task 2	Task 3	Task 4	Task 5
P0	Clock	Clock	Clock*1/32	Clock*1/32	Clock*1/32
P1	Clock*1/16	Clock*2/3	Clock*1/4	Clock*1/16	Clock*1/32
P2	Clock*1/32	Clock*5/32	Clock*1/2	Clock*1/2	Clock*1/32

frequency at the input of the phase detector, non-integer divider such as those in U.S. Pat. No. 6,236,278 can be used as well.

[0045] The controller 140 ensures that the edges of the clock do not generate harmonics that interfere with the 2.4 GHz frequency. In one implementation, the first harmonic of a 1.2 GHz signal is used as the 2.4 GHz carrier frequency. When 2.4 GHz operation is desired, the clock is rapidly increased to 2.4 GHz with a suitable phase locked loop fed to both the processor core and the Bluetooth core. In one implementation, the edges of the clock signal generated by the PLL’s voltage controlled oscillator are phase-modulated using a random-number sequencer in order to reduce the harmonic content of the resulting clock signal. The digital clock can be transformed into an analog carrier wave using a gaussian filter and a lowpass filter such as a high-order Chebyshev or Butterworth filter.

[0046] The CPU performs complex calculations for wireless 802.11a/b transmission, while the Bluetooth transceiver/radio or the 802.11 transceiver/radio is used for local ‘last meter’ transmission of data in a personal area network (PAN). To reduce power consumption, the clock frequency used by the processor core can be less than 2.4 GHz. This can be done by scaling down the 2.4 GHz clock signal with a clock divider. In this manner, a single clocking source can be used for a number of RF and digital operations.

[0047] FIG. 3 shows an exemplary embodiment to conserve power in a system with a plurality of processing elements or units 310, 312, 314, 316 and 318. In this embodiment, processing units 310-312 operate in parallel, while processing units 314, 316, and 318 operate in seriatim based on the previous processing unit’s outputs. Multiple instructions are executed at the same time in the different execution units 310, 312, 314, 316 and 318, as long as these instructions do not contend for the same resources (namely, shared memory). As discussed below, power can be saved by varying the clock frequency, the core voltage or a combination thereof, if necessary, to reduce heat or to reduce battery power consumption.

[0049] The table illustrates a sequence of clock management events in a multiple processing element system. Although the figure indicates all processor clocking management to occur coincidentally, generalization of the invention to include unsynchronized and/or gradual rate changes is a simple extension of the invention. Additionally subsets of processing elements may be grouped and managed together as ensembles.

[0050] The controller 304 can be implemented in hardware; or the power control may be implemented by means of software. If a high performance operating level of the core is not required for a particular application, software instructions may be utilized to operate the power control circuit. In one implementation, switching ability is no longer provided to the processing unit after a preselected clock cycle period after the processing unit has completed the required task of executing the machine code instruction of the computer program to turned off (de-activated) the unit after it has executed the required task.

[0051] FIG. 4 is a block diagram of a second embodiment to conserve power consumption for a plurality of processing units operating in parallel. This embodiment is similar to the embodiment of FIG. 3, except that the output of each of the sequential processing units 314, 316 and 318 is buffered by buffers 324, 326 and 328, respectively. In one embodiment, the buffers 324, 326 and 328 are first-in-first-out (FIFO) buffers.

[0052] FIG. 5 is a block diagram of a third embodiment to conserve power consumption for a plurality of processing units operating in parallel. This embodiment is also similar to the embodiment of FIG. 3, with the addition of a programmable voltage source 330. FIG. 6 is a block diagram of a fourth embodiment similar to the embodiment of FIG. 4, except that the buffered processing units operating in parallel at individually controlled supply voltages. In the embodiments of FIGS. 5-6, each of the processing units 310, 312, 314, 316 and 318 is powered by independent voltage rails whose voltage can be varied within a predetermined range.