source regions are performed after formation of p-type and n-type regions (columns), whereby the mutual impurity diffusion between the p-type and n-type regions (columns) can be suppressed. As such, the invention provides a manufacturing method of a super-junction semiconductor device which can increase the breakdown-voltage-related yield by reducing variations in the impurity dopes of p-type and n-type regions (columns).

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The foregoing advantages and features of the invention will become apparent upon reference to the following detailed description and the accompanying drawings, of which:

[0029] FIGS. **1**A-**1**M are sectional views of important parts of a semiconductor substrate showing part of a manufacturing method of an SJ-MOSFET according to a first embodiment of the present invention;

[0030] FIG. **2**A is a schematic sectional view of a column structure for illustration of a mutual diffusion phenomenon of a conventional SJ-MOSFET;

[0031] FIG. **2**B is a graph of net doping concentration profiles of the conventional SJ-MOSFET of FIG. **2**A; and

[0032] FIG. **3** is a sectional view of an important part of a trench gate SJ-MOSFET according to a second embodiment of the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0033] Manufacturing methods of a super-junction semiconductor device according to embodiments of the present invention will be described hereinafter in detail with reference to the drawings. FIGS. **1**A-**1**M are sectional views of important parts of a semiconductor substrate showing part of a manufacturing method of an SJ-MOSFET according to a first embodiment of the invention. FIG. **3** is a sectional view of an important part of a trench gate SJ-MOSFET according to a second embodiment of the invention. The invention is not limited to the following embodiments as long as it is within the spirit and scope of the invention.

Embodiment 1

[0034] FIGS. **1**A-**1**M are sectional views of important parts of a semiconductor substrate showing part of a manufacturing method of an SJ-MOSFET having a breakdown voltage rating of 600 V. As shown in FIG. **1**A, a wafer having a total thickness of 500 μm is prepared in which a 50-μm-thick n-type epitaxial layer **4** having a phosphorus concentration of 4×10^{15} cm^{-3} is grown on an n-type single crystal silicon substrate (doped with antimony) having a resistivity of 0.01 Ω·cm. Then, a 1.6-μm-thick oxide film **5** is grown by thermal oxidation at 1,100° C. Then, as shown in FIG. **1**B, an oxide film mask is formed by removing 6-μm-wide portions from the oxide film **5** at regular intervals of 6 μm, that is, by performing patterning and etching on an active portion where a main current is to flow. Then, boron ions are implanted (applied to the entire surface) at a dose of 4×10^{14} cm^{-2} and driven at 1,150° C. for 3 hours, whereby 2-μm-deep p-type base regions **6** to become channel forming regions are formed. Then, as shown in FIG. **1**C, phosphorus ions are implanted at a dose of 4×10^{15} cm^{-2} and driven at 1,100° C. for 1 hour, whereby 1-μm-deep n-type source regions **7** are formed.

[0035] In conventional MOSFETs, usually, n-type source regions **7** are formed by implanting arsenic for the following reason. Since arsenic as an n-type dopant has a small diffusion coefficient, it is not prone to move during thermal treatment and hence makes it possible to control the pn junction positions accurately. However, in this embodiment, it is necessary that the pn junctions of n-type source regions **7** and p-type base regions **6** be sufficiently distant from the end portions of mask oxide film **5** directly downward. This is to prevent n-type source regions **7** from being etched away completely by side etching in trench etching of the next step. The use of phosphorus having a larger diffusion coefficient is favorable for making the pn junctions sufficiently distant from the end portions of oxide film **5** directly downward.

[0036] In the example of FIG. **1**C, the depths of p-type base regions **6** and n-type source regions **7** are 2 μm and 1 μm, respectively. Therefore, if it is assumed that p-type base regions **6** and n-type source regions **7** expand parallel with the surface by approximately the same length as in the depth direction, each p-type base region **6** expands horizontally on both sides by about 2 μm under the associated **6**-μm-wide portion of oxide film **5**. Therefore, if the depths of p-type base regions **6** and n-type source regions **7** were set at 3 μm and 2 μm, respectively, in FIG. **1**C, it would be necessary to form the pattern of oxide film **5** in the following manner. That is, the width of oxide film portions is set at 8 μm and the width of exposed portions of the silicon surface between the oxide film portions is set at 8 μm so that adjoining p-type base regions **6** do not contact each other at the surface.

[0037] Subsequently, as shown in FIG. **1**D, trenches **8** of 6 μm in width and 50 μm in depth are formed by etching the silicon wafer by reactive ion etching (RIE) which is highly anisotropic by using the oxide film **5** as a mask. During that course, the thickness of the oxide film **5** is decreased by 0.5 μm to 1.1 μm. Then, as shown in FIG. **1**E, p-type epitaxial silicon **9** is buried in trenches **8** while trichlorosilane, hydrogen, diborane, and hydrogen chloride are supplied simultaneously. As shown in FIG. **1**F, the front surface is planarized by chemical mechanical polishing (CMP) which is stopped when oxide film **5** is exposed. As shown in FIG. **1**G, surface-exposed silicon is etched away, whereby the steps of the silicon surface are reduced in height and the silicon surface is thereby made approximately flat. SJ columns **2** and **3** are formed by the above steps.

[0038] Then, boron ions are implanted at 3×10^{15} cm^{-2} after a resist is applied and patterned. After the resist is removed, annealing is performed at 1,100° C. for 1 hour, whereby high-impurity-concentration second p^+ regions **10** are formed as shown in FIG. **1**H. The high-impurity-concentration second p^+ regions **10** are necessary for increasing the breakdown resistance. After a resist is applied and patterned again, arsenic ions are implanted at 4×10^{15} cm^{-2}. After the resist is removed, driving is performed at 1,100° C. for 1 hour, whereby n^+ source regions **11** which are to contact a source electrode are formed as shown in FIG. **1**I. The n^+ source regions **11** are formed at certain intervals in ladder form (when viewed from above). N^+ source regions **11** are formed to increase the breakdown resistance.

[0039] After oxide film **5** is removed entirely, a known HTO (high temperature oxide) film is grown at a thickness