

## BLOCK REDUNDANCY IMPLEMENTATION IN HEIRARCHICAL RAM'S

### CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of "Block Redundancy Implementation in Heirarchical RAM'S", U.S. application Ser. No. 10/729,405 filed Dec. 5, 2003, which issued as U.S. Pat. No. \_\_\_\_\_, on \_\_\_\_\_, which was a continuation of "Block Redundancy Implementation in Heirarchical RAMS", U.S. application Ser. No. 10/176,843 filed Jun. 21, 2003, which issued as U.S. Pat. No. 6,714,467, on Mar. 30, 2004, which was a continuation-in-part of, and claims benefit of and priority from, application Ser. No. 10/100,757 filed Mar. 19, 2002, titled "Synchronous Controlled, Self-Timed Local SRAM Block", which issued as U.S. Pat. No. 6,646,954 on Nov. 11, 2003 and U.S. application Ser. No. 09/775,701 filed Feb. 2, 2001 which issued as U.S. Pat. No. 6,411,557. The complete subject matter of each of the foregoing applications are incorporated herein by reference in their entirety.

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[0002] [Not Applicable]

### BACKGROUND OF THE INVENTION

[0003] One embodiment of the present invention relates to a programmable device for increasing memory cell and memory architecture design yield. More specifically, one embodiment of the present invention relates to block redundancy adapted to increase design yield in memory architecture.

[0004] Memory architectures typically balance power and device area against speed. High-performance memory architectures place a severe strain on the power and area budgets of the associated systems, particularly where such components are embedded within a VLSI system, such as a digital signal processing system for example. Therefore, it is highly desirable to provide memory architectures that are fast, yet power- and area-efficient.

[0005] Highly integrated, high performance components, such as memory cells for example, require complex fabrication and manufacturing processes. These processes may experience unavoidable parameter variations which may impose physical defects upon the units being produced, or may exploit design vulnerabilities to the extent of rendering the affected units unusable, or substandard.

[0006] In memory architectures, redundancy may be important, as a fabrication flaw or operational failure in the memory architecture may result in the failure of that system. Likewise, process invariant features may be needed to insure that the internal operations of the architecture conform to precise timing and parameter specifications. Lacking redundancy and process invariant features, the actual manufacturing yield for particular memory architecture may be unacceptably low.

[0007] Low-yield memory architectures are particularly unacceptable when embedded within more complex systems, which inherently have more fabrication and manufacturing vulnerabilities. A higher manufacturing yield of the

memory cells may translate into a lower per-unit cost, while a robust design may translate into reliable products having lower operational costs. Thus, it is highly desirable to design components having redundancy and process invariant features wherever possible.

[0008] The aforementioned redundancy aspects of the present invention may can render the hierarchical memory structure less susceptible to incapacitation by defects during fabrication or operation, advantageously providing a memory product that is at once more manufacturable, cost-efficient, and operationally more robust.

[0009] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with the present invention as set forth in the remainder of the present application with reference to the drawings.

### SUMMARY OF THE INVENTION

[0010] The present invention relates to a system and method for providing redundancy in a hierarchically partitioned memory, by replacing small blocks in such memory for example. One embodiment provides such redundancy (i.e., replaces such small blocks) by either shifting predecoded lines or using a modified shifting predecoder circuit in the local predecoder block. Such block redundancy scheme, in accordance with the present invention, does not incur excessive access time or area overhead penalties, making it attractive where the memory subblock size is small.

[0011] One embodiment of the present invention provides a hierarchal memory structure, comprising at least one active predecoder adapted to be shifted out and at least one redundant predecoder adapted to be shifted in.

[0012] One embodiment of the present invention relates to a hierarchical memory structure comprising a synchronously controlled global element, a self-timed local element, and one or more predecoders. In one embodiment, the local element is adapted to interface with the synchronously controlled global element. In such embodiment, at least one predecoder is adapted to fire for current predecoding and at least one predecoder is adapted to fire for previous predecoding. It is further contemplated that a redundant block is adapted to communicate with at least one predecoder.

[0013] Another embodiment of the present invention provides a predecoder block used with a hierarchical memory structure, comprising a plurality of active predecoder adapted to fire for current predecoding and at least one redundant predecoder adapted to fire for previous predecoding. The structure further includes a plurality of higher address predecoded lines and a plurality of lower address predecoded lines, wherein one higher address predecoded line is coupled to all the lower address predecoded lines. At least one shift pointer is included, adapted to shift in the redundant predecoder.

[0014] Yet another embodiment of the present invention provides a predecoder block used with a hierarchical memory structure. The memory structure comprises at least one current predecoder adapted to fire for current address mapping, at least one redundant predecoder adapted to fire for previous address mapping; and shift circuitry adapted to shift the active predecoder out and the redundant predecoder in.