

predecoder **3200C** is shifted out (i.e., becomes inactive) and predecoder **3202E** is shifted in (becomes active) in a domino fashion.

[0235] In another embodiment of the present invention, the predecoded line shifting technique provided previously may be applied to the address lines generating block select signals in a hierarchically partitioned memory, as in DSPM dual port memory architecture for example. FIG. 32 illustrates a local predecoder block **3300** having two predecoders, **3300C** and **3300P**, and a shifting predecoder circuit (not shown) similar to that illustrated in FIG. 34. Additionally, the predecoder **3300** includes a plurality of lines including shift line **3310**, an addrprev line **3312** and addcurrent line **3316**. One of the predecoders (predecoder **3300C** for example) is adapted to fire for “current” address mapping and the other predecoder (predecoder **3300P** for example) is adapted to fire for “previous” address mapping, that is predecoder **3300P** is adapted to fire for an address combination that activates the previous block or predecoder. The fuse shift signal activates the current predecoder **3300C** when shifting is not present for the predecoder block, or the “previous” predecoder **3300P** when shifting is present (i.e., when a predecoder is shifted out).

[0236] More specifically, if there is no signal on line **3310** (i.e., shift line **3310=0**) there is no shifting. Thus addcurrent line **3316** is active and current predecoder **3300C** is used. If there is a defective bit, (current predecoder **3300C** for example), this defective predecoder is shifted out. Shift line **3310** is now active (i.e., shift =1) and the previous predecoder **3300P** is activated using the addrprev line **3312** (i.e., the addresses from the previous predecoder or block). Again, in this embodiment, the predecoders are shifted in a domino fashion.

[0237] FIGS. 33A, 33B & 33C illustrate one embodiment of hierarchical memory architecture comprising a global predecoder **3420**, a global sense amp **3412**, a plurality of cell arrays (cell arrays **3410(0)**, **3410(1)** and **3410(2)** for example), and a plurality of LSA's (LSA's **3413(0)**, **3413(1)** and **3413(2)** for example).

[0238] In this embodiment, the global predecoder **3420** comprises a subset of predecoding circuits or predecoders. The global predecoder **3420** is placed at the intersection of the one or more global x-decoders **3414** and the GSA **3412**. The global predecoder **3420**, in one embodiment, includes the global predecoder circuitry, which forms part of a predecoding tree that doesn't vary much from memory to memory. In this embodiment, the predecoder distribution is optimized so that the allotted area for the memory module is mostly if not entirely filled.

[0239] The local predecoders, generally designated **3422** (comprising predecoders **3422(0)**, **3422(1)**, **3422(2)**, **3422(X)**, **3422(SX)**, **3422(S0)**, **3422(S1)** and **3422(S2)**) are distributed into each subblock at the intersection of the global x-decoder **3414** and the local sense amplifiers **3413** as illustrated. Predecoder line **3402** is illustrated coupled to predecoders **3422(0)**, **3422(1)**, **3422(2)** and **3422(X)**, while predecoder line **3402(S)** is illustrated coupled to predecoders **3422(SX)**, **3422(S0)**, **3422(S1)** and **3422(S2)**. Predecoder line **3402** is active when there is no shifting, while predecoder line **3402(S)** is active when shifted.

[0240] FIG. 33A further illustrates a redundant block **3411**, which in this embodiment comprises a local decoder,

a cell array and a local sense amplifier, where the redundant block communicates with at least one local predecoder. It is contemplated that, while only three cell arrays **3410**, three LSAs **3413**, three GxDEC's **3414**, eight predecoders **3422** and one redundant block **3411** are illustrated, a different number or different combination of the cell arrays, LSAs, GxDECs, predecoders and redundant block are contemplated. Furthermore, this distributed predecoding scheme is self-scaling. As the number of subblocks increase, the needed predecoders are added. Bank decoding is similarly distributed across the global controller block.

[0241] In this embodiment, **3422(0)**, **3422(1)** and **3422(2)** (alternatively referred to as the “current” predecoders) represent the predecoders adapted to be fired or used for “current” address mapping, while predecoders **3422(S0)**, **3422(S1)** and **3422(S2)** (alternatively referred to as the “previous” predecoders) represent the predecoders adapted to be fired or used for “previous” address mapping. If there is a fault in any one of the predecoders, LSAs or cell arrays, the associated shift line activates such that predecoders **3422(0)**, **3422(1)** and **3422(2)** become inactive and predecoders **3422(S0)**, **3422(S1)** and **3422(S2)** become active. FIG. 33B illustrates no shifting (i.e., no fault), when predecoder line **3402**, connected to predecoders **3422(0)**, **3422(1)** and **3422(2)**, is active (the inactive predecoders are designated “IN” in FIG. 33B). FIG. 33C illustrates a fault in the predecoders, LSAs or cell arrays (or some combination), when predecoder line **3402(S)**, connected to predecoders **3422(S0)**, **3422(S1)** and **3422(S2)**, is active (Again the inactive predecoders are designated IN).

[0242] FIG. 34 illustrates a circuit diagram of a local predecoder block similar to that discussed with respect to the embodiment illustrated in FIG. 32. However, it is contemplated that such shift circuit may be used with any of the embodiments provided previously. In the illustrated embodiment, the local predecoder block includes a shifting predecoder circuit for the current block predecoder (no shifting) **3500C** and the shifting predecoder (previous block address inputs) **3500P** in accordance with one embodiment of the present invention.

[0243] Many modifications and variations of the present invention are possible in light of the above teachings. Thus, it is to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as described hereinabove.

1. A hierarchal memory structure, comprising.

- at least one redundant predecoder adapted to be shifted in, for at least one active predecoder of a plurality of active predecoders adapted to be shifted out.

2. The structure of claim 1 further comprising at least one higher address predecoded line coupled to at least said redundant predecoder.

3. The structure of claim 1, further comprising at least one lower address predecoded line coupled to at least one of said plurality of active predecoders and paired with [said] at least one higher address predecoded line.

4. The structure of claim 1, further comprising at least one shift pointer adapted to shift in said redundant predecoder.

5. The structure of claim 1, further comprising shift circuitry adapted to at least shift in said at least one redundant predecoder.