

6. The structure of claim 5, wherein at least one of said active predecoders is adapted to fire for current address mapping.

7. The structure of claim 5, wherein said redundant predecoder is adapted to fire for previous address mapping.

8. The structure of claim 5, further comprising a shift line coupled to at least said shift circuitry.

9. The structure of claim 5, further comprising an addr-current line coupled to at least one of said plurality of active predecoders.

10. The structure of claim 4, further comprising an addr-previous line coupled to at least said redundant predecoder.

11. A hierarchical memory structure comprising:

a synchronously controlled global element;

a self-timed local element interfacing with said synchronously controlled global element;

a plurality of predecoders, wherein at least one of said plurality of predecoders is adapted to fire for current predecoding; and

at least one predecoder being adapted to fire for previous predecoding.

12. The memory structure of claim 11, further comprising a redundant block communicating with at least one predecoder.

13. The memory structure of claim 11, wherein said global element includes a global predecoder.

14. The memory structure of claim 11, wherein said global element comprises at least one global decoder.

15. The memory structure of claim 11, wherein said global element comprises at least one global sense amplifier.

16. The memory structure of claim 11, wherein said local element comprises a plurality of memory cells forming at least one cell array.

17. The memory structure of claim 11, wherein said local element comprises at least one local sense amplifier.

18. The memory structure of claim 11, further comprising at least one predecoder line communicating with at least one of said plurality of predecoders adapted to fire for current predecoding.

19. The memory structure of claim 11, further comprising at least one predecoder line communicating with said predecoder adapted to fire for previous predecoding.

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