the present invention. **FIG. 2** is a cross-sectional view of the power MOSFET taken along the line II-II in **FIG. 1**. In this power MOSFET, a structure within a range having a width B is a single unit structure, which is repeated a plurality of times to form this power MOSPET. This power MOSFET includes an n^+-type substrate **1**, n-type drift regions **2**, p-type silicon regions **3** as first semiconductor regions **3**, p-type base regions **4**, upper n-type silicon regions **5** as second semiconductor regions **5**, n^+-type source regions **6**, and gate electrodes **7**.

[**0022**] The n^+-type substrate **1** forms an n^+-type drain region **1**, and the thickness of the n^+-type substrate **1** is, for example, 2 μm in a vertical direction of the n^+-type substrate **1**. The substrate **1** has a dopant concentration of 1×10^{19} to 1×10^{23} cm^{-3}. The n-type drift regions **2** are located on the n^+-type substrate **1** and have, for example, a dopant concentration of 1×10^{16} to 1×10^{17} cm^{-3}, a width of 1 μm, and a thickness of 10 μm. These values are selected to ensure that the n-type drift regions **2** can be completely depleted when a predetermined reverse voltage is applied.

[**0023**] The n-type drift regions **2** have sidewall surfaces **10***a* and bottom surfaces **10***c* that define first trenches **10**, or epitaxial trenches **10**. The p-type silicon regions **3** are located in the epitaxial trenches **10**. The p-type silicon regions **3** have a dopant concentration of, for example, 1×10^{11} to 1×10^{17} cm^{-3}. The p-type silicon regions **3** have, for example, a width of 3 μm and a thickness of 10 μm. However, the p-type silicon regions **3** have, for example, a width of 1 μm at the portion between the upper n-type silicon regions **5**, which are described later. The aforementioned values are selected to ensure that the p-type silicon regions **3** can be completely depleted when a predetermined reverse voltage is applied.

[**0024**] The n-type drift regions **2** and the p-type silicon regions **3** are arranged alternately in the directions orthogonal to the moving direction of carriers, that is, in the horizontal directions in FIG. **2**. In other words, the n-type drift regions **2** and the p-type silicon regions **3** join at the corresponding pn junctions **10***a*, which are the sidewall surfaces **10***a* of the epitaxial trenches **10**. The pn junctions **10***a* are formed intermittently in horizontal directions by the alternate arrangement of the n-type drift regions **2** and the p-type silicon regions **3**. A so-called super junction **11** is formed by the alternate arrangement of the n-type drift regions **2** and the p-type silicon regions **3**.

[**0025**] The p-type base regions **4** are located on the corresponding p-type silicon regions **3** in direct contact with the p-type silicon region **3**. The p-type base regions **4** have, for example, a dopant concentration of 5×10^{16} cm^{-3} and a thickness of 1.5 μm. A p^+-type base contact region **12** having a thickness of **0.5** am is located on the upper surface of each of the p-type base regions **4**. The upper n-type silicon regions **5** are located between the top surfaces of the n-type drift regions **2** and the lower surfaces of the p-type base regions **4**. The upper n-type silicon regions **5** are in contact with the p-type silicon regions **3** at pn junctions **22**. The upper n-type silicon regions **5** are arranged to include substantially all the carrier passages that connect the n-type drift regions **2** and the p-type base regions **4**.

[**0026**] In this embodiment, the upper n-type silicon regions **5** have, for example, a dopant concentration of 1×10^{16} cm^{-3} which differs from that of the n-type drift regions **2**. However, the dopant concentration of the upper n-type silicon regions **5** may be the same as that of the n-type drift regions **2**. The upper n-type silicon regions **5** are also in contact with the p-type base region **4** at pn junctions **21** and further in contact with n-type channel regions **4***a*, at which n-type channels are formed in the p-type base regions **4**. The upper n-type silicon regions **5** are located between the n-type drift regions **2** and the bottom of second trenches **13**, or gate trenches **13**.

[**0027**] The upper n-type silicon regions **5** are wider than the n-type drift regions **2** and the gate trenches **13**. The upper n-type silicon regions **5** have, for example, a width of 3 μm and a thickness of 1 μm. The upper n-type silicon regions **5** are wider than the n-type drift regions **2** and the gate trenches **13** substantially by the length of the n-type drift region **2** and the gate trenches **13** on both sides in the horizontal directions of **FIG. 2**. The upper n-type silicon regions **5** define the corners **13***a* of the bottom surfaces of the gate trenches **13**.

[**0028**] The n^+-type source regions **6** are in contact with the top surfaces of the p-type base regions **4**. The n^+-type source regions **6** have a thickness of 0.5 μm. The gate electrodes **7** are located on the surfaces of the gate trenches **13**, which extend through the base region **4** from the main surface, with gate oxide films **14**, or gate insulating films **14**, therebetween. In the cross-sectional structure shown in **FIG. 2**, the gate electrodes **7** have, for example, a width of 1 μm and a depth of 2.5 μm. The gate oxide films **14** have a width of 0.1 μm.

[**0029**] Subsequently, the operation of the power MOSFET of this embodiment will be explained. Positive voltage is applied to the n^+-type drain region **1** in **FIG. 2**, and the n^+-type source regions **6** and the p^+-type base contact regions **12** are grounded. When the power MOSFET is turned on in this state, that is, when positive voltage is applied to the trench gate electrodes **7**, electrons in the p-type base regions **4** are drawn to the n-type channel regions **4***a* to form n-type channels. The electrons supplied from the n^+-type source regions **6** flow in the n-type channel regions **4***a*, the upper n-type silicon regions **5**, and the n-type drift regions **2** to reach the n^+-type drain region **1**.

[**0030**] When a reverse voltage is applied between the source electrode and the drain electrode of the power MOSFET of this embodiment with no voltage applied to the trench gate electrodes **7**, that is, while the power MOSFET is in OFF state, depletion layers extend from the pn junctions **10***a* between the n-type drift regions **2** and the p-type silicon regions **3**, the pn junctions **21** between the p-type base region **4** and the upper n-type silicon regions **5**, and the pn junctions **22** between the p-type silicon regions **3** and the upper n-type silicon regions **5** toward each region **2**, **3**, **4**, **5**.

[**0031**] When a predetermined reverse voltage is applied, the n-type drift regions **2**, the p-type silicon regions **3**, and the upper n-type silicon regions **5** are completely depleted. That is, the regions that make up the super junction **11** are completely depleted to permit the power MOSFET to secure high breakdown voltage.

[**0032**] Next, the method for manufacturing the semiconductor device according to this embodiment will be explained. **FIGS. 3A** to **3J** show the steps for manufacturing a semiconductor device according to this embodiment.