

[0026] FIG. 15 is a graph illustrating temperature characteristics of a capacitor according to a second exemplary embodiment of the present invention;

[0027] FIG. 16 is a perspective view illustrating a partial configuration of a semiconductor device according to a second exemplary embodiment of the present invention;

[0028] FIG. 17A is a plan view illustrating a configuration of a semiconductor device according to a third exemplary embodiment of the present invention;

[0029] FIG. 17B is a cross-section taken on line 17b-17b in FIG. 17A;

[0030] FIG. 18 is a functional block diagram illustrating a semiconductor device according to the third exemplary embodiment of the present invention;

[0031] FIG. 19 is a functional block diagram illustrating a semiconductor device according to a fourth exemplary embodiment of the present invention;

[0032] FIG. 20 is a flow chart illustrating a flow of frequency correction processing according to the fourth exemplary embodiment of the present invention;

[0033] FIG. 21 is a functional block diagram of a semiconductor device according to a fifth exemplary embodiment of the present invention;

[0034] FIG. 22 is a flow chart illustrating a flow of frequency correction processing according to the fifth exemplary embodiment of the present invention;

[0035] FIG. 23 is a flow chart illustrating another flow of frequency correction processing according to the fifth exemplary embodiment of the present invention;

[0036] FIG. 24 is a functional block diagram of a semiconductor device according to a sixth exemplary embodiment of the present invention; and

[0037] FIG. 25 is a perspective view illustrating a configuration of a semiconductor module according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0038] Explanation follows regarding exemplary embodiments of the present invention, with reference to the drawings. Note that the same or equivalent configuration elements and portions are allocated with the same reference numerals in each of the drawings.

First Exemplary Embodiment

Configuration of Integrating Electricity Meter

[0039] FIG. 1 is a perspective view of an integrating electricity meter 10 equipped with a semiconductor device 1 (FIG. 2) according to a first exemplary embodiment. The integrating electricity meter 10 is attached to a fixing plate 102 that is fixed to an external wall 100 of for example a house. The integrating electricity meter 10 principally includes: a main body 12; a transparent cover 14 that covers the main body 12; and a connection section 16 provided at a lower portion of the main body 12.

[0040] A power supply-side cable 18 and a load-side cable 20 are connected from below the connection section 16 and supply current to the integrating electricity meter 10. The main body 12 is a box body of rectangular shape when viewed face on (referred to below as plan view). The semiconductor device 1 and a power consumption metering circuit 22 are mounted on a base plate inside the main body 12. The power consumption metering circuit 22 serves as a metering section

that generates timing data based on a measuring signal output from the semiconductor device 1 and measures integral power consumption associated with the timing data. Namely, the power consumption metering circuit 22 meters power consumption per unit time and integral power consumption for each separated time band. A liquid crystal display 15 is provided with its length aligned in a transverse direction on the front face of the main body 12. The liquid crystal display 15 displays such information as the power consumption per unit time as measured by the power consumption metering circuit 22 and the integral power consumption used in each time band. Note that although the integrating electricity meter 10 according to the present exemplary embodiment is an electronic electricity meter in which the power consumption metering circuit 22 is employed as the metering section, there is no limitation thereto. A rotating disk induction type electricity meter may for example be employed for measuring the power consumption. Moreover, although an explanation is given in the present exemplary embodiment of an example of the integrating electricity meter 10 that performs metering of power consumption as a metering device, a device may be employed that meters another metering commodity associated against time data other than electricity, such as for example water or gas.

[0041] Semiconductor Device Structure

[0042] FIG. 2 is a plan view illustrating a configuration of the semiconductor device 1 according to a first exemplary embodiment of the present invention, FIG. 3 is a cross-section taken on line 3-3 of FIG. 2. Note that in the FIG. 2 the left-right direction is the arrow X direction, and the up-down direction is the arrow Y direction, and the Z direction is a direction orthogonal to the X-Y plane. The external shape of the semiconductor device 1 is a rectangular shape in plan view, and the semiconductor device 1 includes a lead frame 26 that acts as a framework, a temperature sensing device (temperature sensor) 27 and an oscillator 28 mounted to a first main face 25A of a die pad 26A configuring the lead frame 26, a semiconductor chip 30 that is mounted to a second main face 25B of the lead frame 26 on the opposite side to the first main face 25A of the die pad 26A, and molding resin 32 that serves as a sealing member for these members mounted on the die pad 26A.

[0043] The lead frame 26 is a plate member formed from a flat sheet of a metal such as copper (Cu) or an iron (Fe) and nickel (Ni) alloy, by pressing out with a press. The lead frame 26 includes: a die pad 26A provided at a central portion; hanging leads 26B that extend outwards from the die pad 26A along diagonal lines; and plural leads (terminals) 38 provided between adjacent of the hanging leads 26B.

[0044] The leads 38 are long thin members extending towards a central portion of the die pad 26A, with plural of the leads 38 formed at a specific separation around the periphery of the die pad 26A. In the present exemplary embodiment there are 16 lines of the leads 38 formed between each adjacent pair of the hanging leads 26B. The leads 38 are configured from inner leads 38A that are positioned on the die pad 26A side and are buried in within molding resin 32, and outer leads 38B that are positioned at the outer peripheral end side of the semiconductor device 1 and exposed from the molding resin 32. The inner leads 38A are pressed down by a press so as to be lower than the die pad 26A and extend parallel to the die pad 26A (see FIG. 3). The leading end portions of the inner leads 38A nearest to the die pad 26A are covered with an electroplated film 40. In the present exemplary embodiment,