disposed to support layers 'b'-'e', for example contact **8** may comprise a thick contact material. Second layer 'b' may be disposed on and/or adjacent to first layer 'a', the third layer 'c' may be disposed on and/or adjacent to second layer 'b', fourth layer 'd' may be disposed on and/or adjacent to third layer 'c', and fifth layer 'e' may be disposed on and/or adjacent to fourth layer 'd'. In at least one aspect, photovoltaic device **70** has substrate **9** in layer 'f' and fifth layer 'e' may dispose and/or be adjacent with fourth layer 'd'. Each layer may be deposited on an adjacent layer. For example, contact **8** may be deposited substrate **9**, semiconductor **6** may be deposited on contact **8**, insulator **11** may be deposited on semiconductor **6**, contact **4** may be deposited on insulator **11**, and absorber **2** may be deposited on contact **4**.

[0074] FIG. **7***a* shows a top view of photovoltaic device **70** having absorber **2** removed therefrom. In this respect, a portion of layer 'd' is shown having contact material **4** and a portion of layer 'b' is shown having first semiconductor **6**. In this aspect, electrode or contact material **4** may comprise an array of holes in a sheet, forming the second electrode or contact **4**, and insulator **11** may be similarly shaped.

[0075] Thin film photovoltaic device **70** with back contacts **8** and **4** comprises a first contact **8** disposed in first layer 'a' and has an upper surface and a lower surface. Semiconductor **6** is disposed in second layer 'b' and has a lower surface disposed on the upper surface of the first contact **8**. An insulator **11** is disposed in a third layer 'c' and on an upper surface of the semiconductor **6**. Second contact **4** is disposed in a fourth layer 'd' and solely on insulator **11**. Absorber **2** completely fills fifth layer 'e' and is disposed about second contact **4** and insulator **11**. Second layer 'b' may be adjacent first layer 'a', third layer 'c' may be adjacent second layer 'b', fourth layer 'd' may be adjacent third layer 'c', and fifth layer 'e' may be adjacent fourth layer 'd'.

[0076] Absorber **2** of photovoltaic device **70** may comprise a p-type semiconductor or a n-type conductor and semiconductor **6** may comprise the other of the p-type semiconductor and n-type conductor. Insulator **11** may be disposed in third layer 'c' and may be configured to insulate against direct electrical communication between semiconductor **6** and second contact **4** and ensure electrical communication between first contact **8** and second contact **4** occurs solely through semiconductor **6** and absorber **2**. Photovoltaic device **70** may comprise substrate **9** and first contact **8** may be have its lower surface disposed on substrate **9**. Second contact **4** may have an interrupted pattern and thereby only partially filling fourth layer 'd' and absorber **2** may fill the interrupts in second contact **4**.

[0077] Photovoltaic device **70** may comprise a first electrode **8** disposed in first layer 'a', semiconductor **6** disposed in second layer 'b' on first electrode **8**, insulator **11** may have an interrupted pattern and may be disposed in third layer 'c' on semiconductor **6**, second electrode **4** may be disposed in fourth layer 'd' and only on insulator **11**, absorber **2** may entirely fill fifth layer 'e' and be disposed on second electrode **4** and may fill the interrupted patterns of insulator **11** and second electrode **4**. Insulator **11** may be comprised of a non-conducting or non-semiconducting materials. For example, insulator **11** may consist of SiO_2. Absorber **2** may comprise a p-type semiconductor or a n-type conductor and semiconductor **6** may comprise the other of the p-type semiconductor and n-type conductor. The p-type material may be selected from the group consisting of: cadmium telluride, copper indium diselenide, copper indium gallium diselenide and copper oxide. The p-type material may be doped or undoped. The n-type material may be either cadmium sulfide or zinc oxide, and may be doped or undoped.

[0078] FIG. **8** shows a scanning electron microscope image of a cross-section of a photovoltaic device of the present disclosure. For example, the aspect of the present disclosure may have a configuration similar to photovoltaic devices **40** or **70**. Semiconductor **6** is disposed on an upper surface of a first contact **8**, not shown. Insulator **11** is disposed on an upper surface of semiconductor **6**. Second contact **4** is disposed on insulator **11**. Absorber **2** surrounds or encases contact **4**, insulator **11**, and semiconductor **6**.

[0079] FIG. **9** shows a scanning electron microscope image of a cross-section of a photovoltaic device of the present disclosure. For example, the aspect of the present disclosure may show a configuration similar to photovoltaic device **10**. First contact **8** is shown disposed on an upper surface of substrate **9**. Semiconductor **6** is disposed on an upper surface of the first contact **8**. Absorber **2** is disposed on an upper surface of semiconductor **6**. Second contact **4** is disposed on a portion of absorber **2** and absorber **2** surrounds or encases contact **4** and semiconductor **6**. Electrical communication between first contact **8** and second contact **4** is solely through absorber **2** and semiconductor **6**.

[0080] FIG. **10** shows a plot of External Quantum Efficiency, specifically the % of light converted and captured as electrical current across the contacts **4** and **8**, versus the energy of the light photons impinging on the CdS absorber **2** of the device, the light energy measured in electron volts eV, for an aspect of the present disclosure having an absorber comprising CdS. The transition from zero to nonzero fraction of light converted into electrical current at energies greater than ~2.4 eV is an unambiguous signature of light absorbed in the CdS absorber as the CdS bandgap is approximately this value. Aspects of the present disclosure may be made by depositing a bottom electrode in planar form, for example by thin film deposition processes. The electrode may be deposited on a substrate. A semiconductor may then be deposited on the electrode. An insulator, second semiconductor, or first amount of an absorber may then be deposited on the semiconductor. A second electrode may then be deposited on the insulator, second semiconductor, or first amount of an absorber. An absorber, or second amount thereof, may then be deposited on the second electrode. The second electrode may be interrupted or otherwise not completely filling its layer. For example, the second electrode may be in the form of a plurality of wires or may have holes. In this aspect, the absorber, or second amount thereof, fills the interruptions in the second electrode and completely covers the electrode, forming an outer layer that is solely comprised of the absorber. The use of an interrupted, or embedded patterned electrode, may eliminate upper surface contacts and allow full illumination of most of the absorber.

[0081] Aspects of the present disclosure may be made by depositing a bottom conductor or using a conducting substrate. A first amount of a semiconducting material may be deposited on the bottom conductor. A different semiconducting material may then be deposited on the first amount of semiconducting material. A second electrode may be patterned and deposited on the semiconducting materials. The absorber may then be deposited to fill the pattern and cover the second electrode. Deposition may by any process as is known in the art. For example, a thin film deposition process such as sputtering, chemical vapor deposition (CVD), chemi-