

means does not perform reading-in of operating device data each time it uses operating device data, but the operating device data is processed by a means other than the central processing means. It is accordingly possible to realize a game machine in which the amount of processing required by the central processing means is reduced to secure more time for game processing.

[0013] Also, operating device data is stored in a memory means that also stores other data required for advancing a game so that the central processing means is allowed to process operating device data similarly to other game data. Therefore the central processing means can perform game processing at high speed and with high freedom.

[0014] Furthermore, according to one aspect of the present invention, operating device data can be partially read and accordingly there is no necessity of reading operating device data in its entirety at one time. Therefore unwanted portions of operating device data can be left unread, shortening read-in speed.

[0015] According to another aspect, it is possible to store data to be processed by the central processing means into an expansion device such as extension memory connected to the operating device. The expansion device may alternatively be a liquid crystal display.

[0016] According to another aspect, it is possible to load the data stored in an extension memory connected to one of a plurality of operating devices into an extension memory connected to another operating device. This enables exchanging of data between players.

[0017] Furthermore, according to another aspect, the data in an external memory means is temporarily stored in the operation storing means so that data conversion and copying is possible by the central processing means. This enables data to be copied in a different format than respective external memory means.

[0018] The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 is a block diagram showing an exemplary conventional video game system;

[0020] FIG. 2 is an illustrative external view showing one embodiment of an exemplary video game system;

[0021] FIG. 3 is an exemplary block diagram showing a game machine in the FIG. 2 embodiment;

[0022] FIG. 4 is an illustrative view showing a CPU memory map of the FIG. 3 embodiment, showing an external memory and a W-RAM address space incorporated in a cartridge;

[0023] FIG. 5 is a block diagram showing of an exemplary controller control circuit in the FIG. 3 embodiment;

[0024] FIG. 6 is an illustrative view showing controller data illustrating a modulating/demodulating method for such data;

[0025] FIG. 7 is an illustrative view showing an exemplary memory map of a RAM in FIG. 5;

[0026] FIG. 8 is a perspective view of a controller of FIG. 3 embodiment as viewed from the top;

[0027] FIG. 9 is perspective view of the controller of FIG. 3 embodiment as viewed from the bottom;

[0028] FIG. 10 is a perspective view of showing an analog joystick unit capable of being utilized in the embodiment;

[0029] FIG. 11 is a perspective view showing major portions of the FIG. 10 unit;

[0030] FIG. 12 is an exploded perspective view showing major portions of the FIG. 10 unit;

[0031] FIG. 13 is a sectional illustrative view showing major portions of the FIG. 10 unit;

[0032] FIG. 14 is a block diagram showing in detail one example of the controller and an expansion device;

[0033] FIG. 15 shows illustrative data of the analog joystick and respective buttons of the controller;

[0034] FIG. 16 is a block diagram showing in detail another example of the controller and an expansion device;

[0035] FIG. 17 is a flowchart showing operation of the CPU of FIG. 3 embodiment;

[0036] FIG. 18 is a flowchart showing operation of the bus control circuit of the FIG. 3 embodiment;

[0037] FIG. 19 is a flowchart showing operation of the controller control circuit of FIG. 3 embodiment;

[0038] FIG. 20 is flowchart showing operation of the controller circuit of FIG. 3 embodiment;

[0039] FIG. 21 is an illustrative view of transmission and reception data by the control circuit when a command "0" is transmitted from the controller control circuit;

[0040] FIG. 22 is an illustrative view of transmission and reception data by the control circuit when a command "1" is transmitted from the controller control circuit;

[0041] FIG. 23 is an illustrative view of transmission and reception data by the control circuit when a command "2" is transmitted from the controller control circuit;

[0042] FIG. 24 is an illustrative view of transmission and reception data by the control circuit when a command "3" is transmitted from the controller control circuit;

[0043] FIG. 25 is an illustrative view of transmission and reception data by the control circuit when a command "255" is transmitted from the controller control circuit;

[0044] FIG. 26 is a flowchart showing a data copy operation;

[0045] FIG. 27 is a flowchart showing a first method of origin point resetting;

[0046] FIG. 28 is a flowchart showing a second method of origin point resetting;

[0047] FIG. 29 is an illustrative view showing the correspondence of a physical coordinate of the joystick to a display screen;