

[0048] FIG. 30 is an illustrative view showing the correspondence of the physical coordinate of the joystick to the display screen when resetting an origin point.

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[0049] FIG. 2 is an exemplary illustration showing a game machine system according to one illustrative embodiment of the present invention. The game machine system is, for example, a video game machine system, which inclusively comprises a game machine 10, a ROM cartridge 20 (as one example of an external memory device), a monitor 30 (as one example of a display means) connected to the game machine 10, a controller 40 (as one example of a player controller operating device), and a RAM cartridge 50, as one example of an extension device detachably attached to the controller 40. The external memory device stores image data and program data for image processing for games, and audio data for music, sound effects, etc. A CD-ROM or a magnetic disc may alternatively be employed in place of the ROM cartridge. Where the game machine system of this example is applied to a personal computer, an input device such as a keyboard or a mouse is used as the player operating device.

[0050] FIG. 3 is a block diagram of the game machine system of this example. The game machine 10 incorporates therein a central processor unit (hereinafter "CPU") 11 and a bus control processing circuit 12. The bus control processing circuit 12 is connected to a cartridge connector 13 for detachably attaching the ROM cartridge 20, as well as a working RAM 14. The bus control processing circuit 12 is connected to an audio signal generating circuit 15 for outputting an audio signal processed by the CPU 11 and a video signal generating circuit 16 for outputting a video signal, and further with a controller control circuit 17 for serially transferring operating data of one or a plurality of controller(s) 40 and/or data from RAM cartridge(s) 50. The controller control circuit 17 is connected with controller connectors (hereinafter abbreviated as "connectors") 181-184 which are provided at a front face of the game machine 10. To the connector 18 is detachably connected a connection jack 41 and the controller 40 through a cable 42. Thus, the connection of the controller to the connector 181-184 places the controller 40 into electric connection to the game machine 10, enabling transmission and reception of data therebetween.

[0051] More specifically, the bus control processing circuit 12 inputs commands output as parallel signals from CPU 11 via a bus, performs parallel to serial conversion, outputs command as serial signals to the controller control circuit 17, and converts serial signal data input from the controller control circuit 17 into parallel signals and output such signals to the bus. The data output through the bus is subject to processing by CPU 11, or is stored in W-RAM 14. The W-RAM 14 is a memory temporary storing data to be processed by CPU 11, wherein read-out and write-in of data is possible through the bus control circuit 12.

[0052] FIG. 4 is a diagrammatic illustration showing memory regions assigned to respective memory spaces. The memory spaces accessible by the CPU via the bus control processing circuit 12 involves an external memory address space of the ROM cartridge 20 and a memory address space of the W-RAM 14. The ROM cartridge 20 is structured by mounting on a board a ROM stored with data for game

processing and accommodating the same board in a housing. The ROM storage data is shown by the external memory region shown in FIG. 4. The ROM includes an image data storage region 201 for storing image data required to cause the game machine 10 to generate image signals for the game, and a program data region 202 for storing program data required for predetermined operation of the CPU 11. In the program data region 202, there are stored an image display program for performing image display processing based on image data 201, a time-measuring program for carrying out measurement of time, and a determination program for determining that the cartridge 20 and an extension expansion device 50, are in a predetermined relationship. The details of the time-measuring program and the determination programs are described below. The memory region of W-RAM 14 includes a controller data region 141 for temporarily storing data representative of an operating state from a control panel.

[0053] FIG. 5 is a more detailed circuit diagram of a controller control circuit 17. The controller control circuit 17 transmits and receives data in serial form to and from the bus control processing circuit 12 and the controller connectors 181-184, and includes a data transfer control circuit 171, a signal transmitting circuit 172, a signal receiving circuit 173 and a RAM 174 for temporarily storing transmission and reception data. The data transfer control circuit 171 includes a parallel-serial conversion circuit and a serial-parallel conversion circuit for conversion of data format during data transfer, and also performs control of write-in and read-out of the RAM 174. The above-mentioned serial-parallel conversion circuit converts serial data supplied from the bus control processing circuit 12 into parallel data to provide such data to the RAM 174 or the signal transmitting circuit 172. The parallel-serial conversion circuit converts parallel data supplied from the RAM 174 or the signal receiving circuit 173 into serial data to provide such data to the bus control processing circuit 12. The signal transmission circuit 172 converts parallel data for signal read-in control of the controller 40 supplied from the data transfer control circuit 171 and write-in data (parallel data) to the RAM cartridge 50 into serial data, which serial data is transmitted through a corresponding channel CH1-CH4 to each of the plurality of controllers 40. The signal receiving circuit 173 receives serial read-out data, representative of an operating state of each of the controller 40, input through a corresponding channel CH1-CH4 to each of the controller 40 as well as read-out data from the RAM cartridge 50, to convert such data into parallel data to provide it to the data transfer control circuit 171.

[0054] The signal transmitting circuit 172 and the signal receiving circuit 173 in the exemplary embodiment adopt a duty-cycle modulation and demodulation (hereinafter referred to as "modulation/demodulation") method as one example of the modulation/demodulation method that may be employed here. The duty-cycle modulation/demodulation method, as shown in FIG. 6, is a modulation/demodulation method wherein "1" and "0" are represented by varying a Hi time period and a Lo time period for a signal at a certain interval. Explaining the modulation/demodulation method in more detail, when data to be transmitted in serial is a logical "1", a signal having, within one cycle period T, a high-level period tH rendered longer than a low-level period tL (tH>tL) is transmitted. When data to be transmitted is a