

command is a pad-data request command (command "1"). If it is a command "1", the process proceeds to a step S55 where the process of transmitting pad data is performed. Specifically, where the CPU 11 outputs a command "1", the data in format as shown in FIG. 14 is transmitted and received between the game machine 10 and the controller 40. On this occasion, the control circuit 442, if receiving command "1" data configured by 1 byte (8 bits), transmits the data of 14 switches (16 bits) of B, A, G, START, upper, lower, left, right, L, R, E, D, C and F, the data of JSRST (1 bit); and the data of the counter 444X and the counter 444Y (16 bits). By transmitting these data to the game machine 10, the game machine 10 recognizes how the operator operated the controller 40. Thus, these data are utilized for modifying the image by the game machine 10 in accordance with the operating state of the controller 40 as manipulated by the player.

[0094] At the foresaid step S54, if the determination reveals that there is not a command "1", it is determined at step S56 whether or not the input command is a read-out request command (command "2") for data associated with the RAM cartridge 50 to be connected to the extension connector. If it is a command "2", the process proceeds to a step S57 where the process of reading out of the extension connector is performed. Specifically, where the CPU 11 outputs a command "2", the data in format as shown in FIG. 13 is transmitted and received between the game machine 10 and the controller 40. On this occasion, when the control circuit 442 receives command "2" data configured by 1 byte (8 bits), address H representative of the higher-order bits (8 bits) of address, address L representative of the lower-order bits (3 bits) of address, and address CRC (5 bits) for checking for error in address data transmitted and received, the control circuit 442 transmits data stored in the RAM cartridge (32 bytes) and CRC (8 bits) for checking for data errors. In this manner, the connection of the RAM cartridge 50 (or other extension devices) and the game machine 10 enables the game machine 10 to process data from the RAM cartridge 50, etc.

[0095] At the aforesaid step S56, if the determination is not a command "2", it is determined at a subsequent step S58 whether or not the inputted command is write-in request command (command "3") for information associated with the RAM cartridge 50 being connected to the extension connector 46. Where it is the command F "3", the process of data read-out is carried out at a step S59 for the RAM cartridge 50 being connected to the extension connector 46. Specifically, if the CPU 11 outputs a command "3", the data shown in FIG. 23 is transmitted and received, in response to the command "3", between the game machine 10 and the controller 40.

[0096] That is, when the control circuit 442 receives command "3" data configured by 1 byte (8 bits), address H representative of the higher-order bits of address (8 bits), address L representative of the lower-order bits of address (3 bits), address CRC for checking for error in address data transmitted and received (5 bits), and data to be transmitted to the RAM cartridge 50 (32 bytes), it transmits CRC for checking for error for data received (8 bits). In this manner, the connection of the extension device 50 and the game machine 10 enables the game machine 10 to control the

extension device 50. The connection of the extension device 50 and the game machine 10 also drastically improves the function of the controller 40.

[0097] If at the aforesaid step S58 the determination is not a command "3", it is determined at a step S60 whether or not it is a reset command (command 255). Where it is the reset command (255), the process of resetting the counter 444 for the joystick 45 is performed at step S61.

[0098] Where the CPU 11 outputs a reset command (command 255), the data shown in FIG. 25 is transmitted and received between the game machine 10 and the controller 40. That is, the control circuit 442 of the controller 40, if receiving command 255 data configured by 1 byte (8 bits), outputs a reset signal to reset the X counter 444X and counter 444Y and transmits aforesaid TYPE L (1 byte), TYPE H (1 byte) and the status.

[0099] The operation by the controller control circuit 17 of transferring data will be explained using the flowchart in FIG. 26, wherein the data, stored in a RAM 51 within an extension device 50 connected to a joy port connector 46 of a controller 40 (controller A) having a connection jack 41 connected to the controller connector 181 is transferred to a RAM 51 within an extension device 50 connected to a joy port connector 46 of a controller (controller B) having a connection jack 41 connected to the controller connector 182.

[0100] First, if the operator operates the controller 40 to determine commencement of backup or if the start of a copying operation is determined by the program, the data transfer control circuit 171 transmits a command "2" to the controller A at a step S191. The controller A performs a predetermined operation in accordance with the command "2" to transfer the data stored in the RAM 51 to the data transfer control circuit 171. At a step S193, the data transfer control circuit 171 stores the data received from the controller A to the RAM 174. At a step S194 the data transfer control circuit 171 transfers the data stored in the RAM 174 to the W-RAM 14. When the data format is different between the RAM 51 connected to the controller A and the RAM 51 connected to the controller B, the data stored in the W-RAM 14 is altered by the CPU 11. At a step S195 the data transfer control circuit 171 transfers the data stored in the W-RAM 14 to the RAM 174. At a step S197, the data transfer control circuit 171 transmits a command "3" to the controller B. At a step S196, the data transfer control circuit 171 transmits the data stored in the RAM 174 to the controller B. At a step S198, it is determined whether or not the data to be transferred from the controller A to the controller B have all been transferred. If the transfer is completed, the backup operation is ended. Where the transfer is not completed, the step S191 through the step S198 are executed again.

[0101] By executing the step S191 through the step S198 in this manner, it is possible to store the data stored in the RAM 51 of the extension device 50 connected to the controller A to the RAM 51 of the extension device 50 connected to the controller B.

[0102] By so doing, it is possible to analyze a competition record of a competitor for future battle references. Even when a racing game or a baseball game is played alone, it is possible to compete with a competitor's machine or baseball team by using machine tuning data or baseball team data of a competitor.